

METHODS AND SYSTEMS FOR DETECTING MEMORY ADDRESS TRANSFER ERRORS IN AN ADDRESS BUS

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ABSTRACT OF THE DISCLOSURE

A method for detecting transfer errors in an address bus is provided. In this method, a first address parity is generated using a memory address. Next, at least two data error-correction-code (ECC) check bits are scrambled using the first address parity. Subsequently, the data ECC check bits are written to a memory and the data ECC check bits enable
10 detection of transfer errors in the address bus. A system for detecting transfer errors in an address bus is also described.